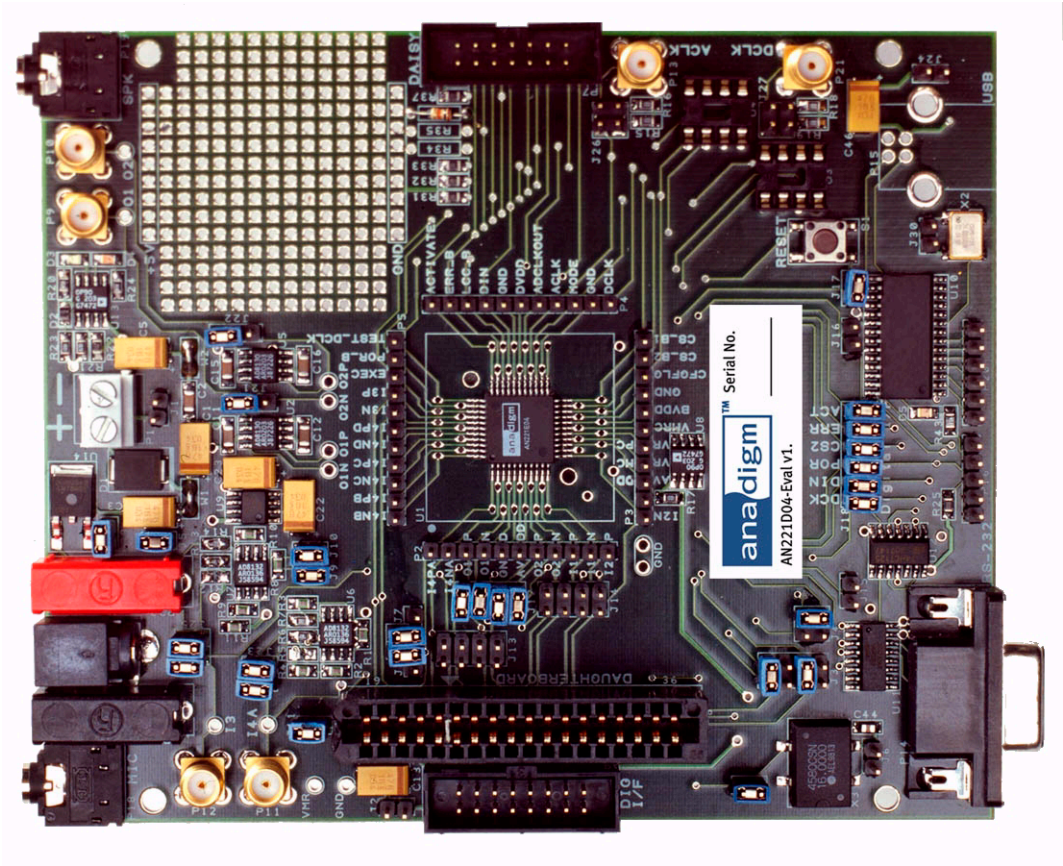
Anadigmvortex AN221D04
Evaluation Board User Manual

The Anadigmvortex evaluation board is designed to help you quickly get started with developing and testing your analog designs; using Anadigm®'s latest Field Programmable Analog Array (FPAA) platform - the AN221E04 device.

This evaluation board comprises of a single AN221E04 device that can be configured from a PC running the AnadigmDesigner®2 software or by using an on-board EPROM or via the user's own digital system. The input signal can be presented via SMA connectors (single-ended ground referenced signals), or via a stereo jack from an audio source. The output is also available via the SMA output connectors or via a stereo output - speakers/headphones. All AN221E04 FPAA input and output signals can be accessed directly via header pins.

The number of devices can be expanded using a daughter card and/or by daisy chaining two or more evaluation boards.

In summary, this system is designed to be very flexible and allows you to fully exercise all the features and capabilities of the AN221E04 device - the innovative new FPAA solution from Anadigm®!



This evaluation board is designed to be used to evaluate the latest Anadigm® FPAA only. Do not use this board to characterize the specifications of the AN221E04 silicon. The evaluation board with all associated circuitry, traces and jumpers is not an ideal characterization platform.

To accurately characterize the AN221E04 silicon in your application, please contact Anadigm® sales or distributors to purchase sample devices; and mount these on your system board.

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In order to assure compatibility, please make sure to use AnadigmDesigner®2 version 2.2.7 (or later). This will guarantee that designs will be fully compatible with the AN221D04 evaluation board. All previous versions of AnadigmDesigner®2 software will NOT work with this board.

With the new AnadigmDesigner®2 version 2.2.7 (or later) designs done for the AN120E04, AN121E04 or the AN220E04 device can all be evaluated the AN221D04 evaluation board. The software (version 2.2.7 or later) will allow designs done for any of Anadigm devices to be evaluated on the AN221D04 platform.

1 Getting Started – Anadigmvortex Evaluation Board 1
1.1 Powering Up the Evaluation Board ... 2
Regulated 5 VDC Supply: ... 2
9 VDC Wall Converter (US 120 VAC Only): ... 2
Powered by a Host System: ... 2
1.2 Configuring the Evaluation Board ... 2
1.3 Using the I/O on the Evaluation Board ... 4
1.4 Using the Daughter Card ... 7
1.5 Expanding the Evaluation Board ... 8

2 Jumper Settings 9
Table 1 — Jumper Function and Default Settings ... 10
J1 - Schottky Bypass ... 11
J2 - Power from Digital Board ... 11
J3 - Multi Device Chain Configuration ... 11
J4 - Clock Configuration ... 11
J5 - Analog Circuitry Power ... 12
J6 - ACLK/SPIP 16 MHz Oscillator Module Disable ... 12
J7, J8 - S2D Converter to I4PA & I4NA ... 12
J9, J10 - S2D Converter to I3P & I3N ... 13
J11 - Select Buffered VMR ... 13
J12, 13, 14 - Output Select to D2S ... 13
J15 - EPROM Mode Motherboard ... 13
J16 - Test Mode ... 13
J17 - CS1b First Device ... 14
J18 - Digital Interface ... 14
J21 - SMA Output Socket P9 ... 14
J22 - SMA Output Socket P10 ... 14
J23 - 50 ohm on Analog Input 4A ... 14
J25 - 50 ohm on Analog Input 3 ... 14
J26 - 50/100 ohm on External ACLK/SPIP Input ... 14
J27 - 50/100 ohm on External DCLK Input ... 14
J28 - Unregulated Power Supply ... 14
J29 - 16 MHz Oscillator Module to ACLK/SPIP ... 15
J30 - Disable PIC Clock ... 15
J31, J32 - Connect P11 & P12 to S2D Converters ... 15
R48, R49 - DCLK Source ... 15

3 Typical Board Configurations 16
Default State Setting ... 17
EPROM Mode Setting ... 17
External Digital Interface Setting ... 17
No Analog Circuitry Setting ... 17
Daughter Card Only - 2 Devices Setting ... 17
Daughter Card + Motherboard - 3 Devices Setting ... 17
External Clocks Setting ... 17
Expanded Board - First board ... 17
Expanded Board - Last board ... 17

4 Electrical and Mechanical Specifications 18
4.1 Absolute Maximum Ratings ... 18
4.2 Recommended Operation Conditions ... 19
4.3 Power Consumption ... 19
4.4 Mechanical ... 20

Appendix – Evaluation Board Schematics 21

Getting Started – Anadigmvortex Evaluation Board

Figure 1 – Different Headers, Power Plugs, Inputs, and Outputs on the Anadigmvortex Evaluation Board 1
Figure 2 – Multiple FPAAs Configured from a Single SPI EEPROM 3
Figure 3 – Multiple FPAAs Configured from a Single FPGA EEPROM 3
Figure 4 – A single FPAA Device with a Sample SPI EEPROM 4
Figure 5 – A single FPAA Device with a Sample FPGA EEPROM 4
Figure 6 – Single-Ended to Differential Converters 5
Figure 7 – Differential to Single-Ended Converters 6
Figure 8 – Digital Signal Connections on Daughter Card 7
Figure 9 – Daughter Card to Motherboard Analog Connections 8

Jumper Settings

Figure 10 – Position of all the Jumpers On Board 9
Figure 11 – J3 Jumper Settings for Different Chain Configurations 11
Figure 12 – J4 Jumper Settings for Clock Configuration 12
Figure 13 – Analog Signal Routing 13

Electrical and Mechanical Specifications

Figure 14 – Mechanical Outline for the AN221D04 Motherboard 20

1 Getting Started – Anadigmvortex Evaluation Board

First of all, familiarize yourself with the different headers, power plugs, inputs, and outputs on this versatile board - shown in Figure 1.

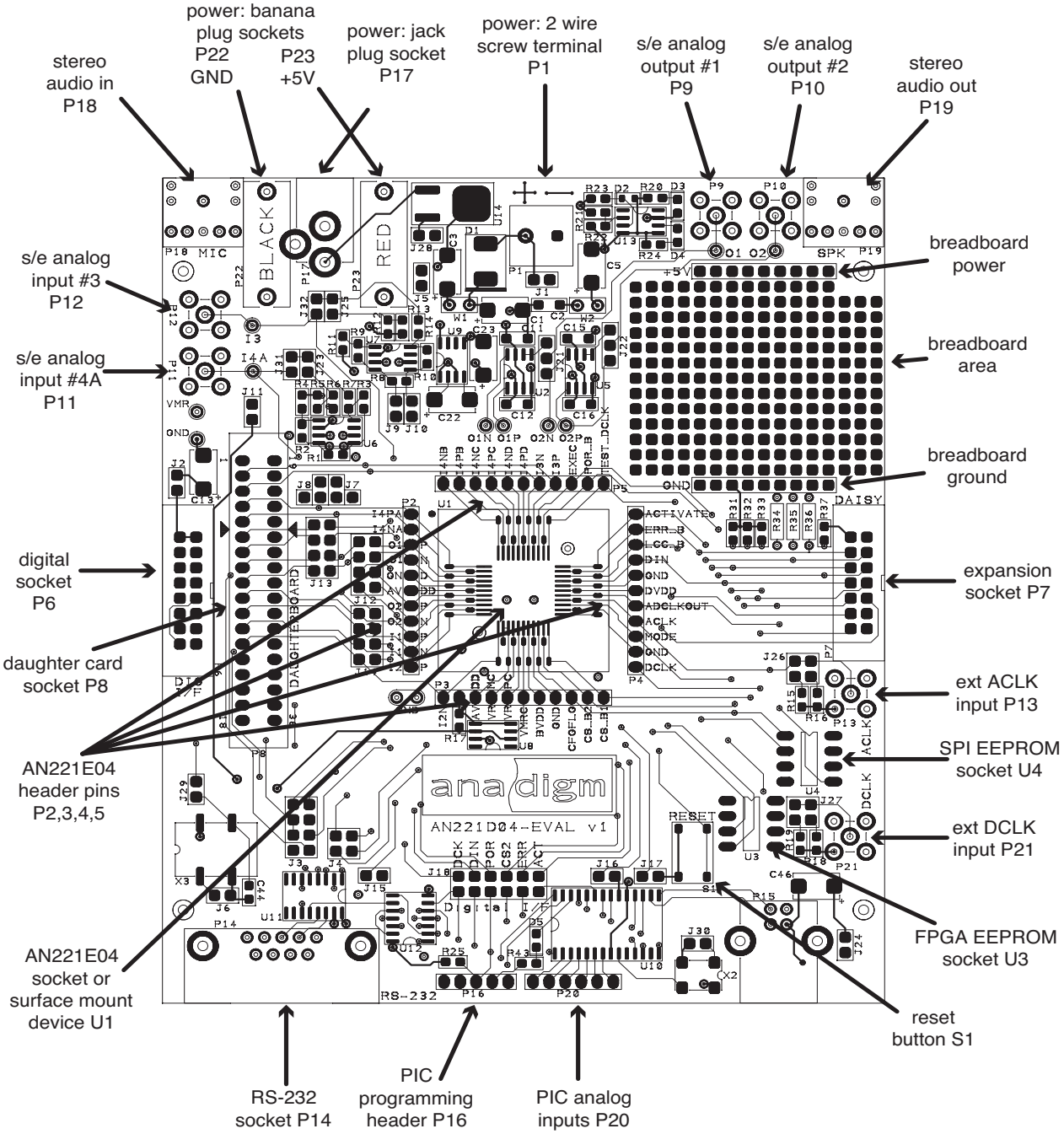


Figure 1 – Different Headers, Power Plugs, Inputs, and Outputs on the Anadigmvortex Evaluation Board

Make sure that you are using AnadigmDesigner version 2.2.7 (or later version) to download your design to the AN221D04 evaluation board. All previous versions of the AnadigmDesigner2 software will NOT work with this board. Also designs done for the AN120E04, AN121E04 or the AN220E04 device can all be evaluated this new board. The software (version 2.2.7 or later) will allow designs done for any of Anadigm devices to be evaluated on the AN221D04 platform.

1.1 Powering Up the Evaluation Board

There are two means of providing power to the evaluation board. One is using a regulated 5 V supply. The other is via the unregulated AC supply. In the second case, a standard AC to 9 VDC converter must be used. By default the evaluation board is configured to be powered up using a 9 VDC wall converter.

The Anadigmvortex evaluation board may be powered using the following methods:

Regulated 5 VDC Supply:

1. Connect a twisted wire pair from a regulated 5 V supply to the 2 wire screw terminal block P1.

OR

2. Connect a pair of banana plug leads from a regulated 5 V supply to the banana plug sockets P22 (GND) and P23 (+5 V).

Remember use option 1 OR option 2; NOT both at the same time.

There is a Schottky diode in series with the supply when using either the screw terminal block P1 or the banana plug sockets P22 and P23. This protection diode drops about 0.2 V. If you wish to bypass this diode, place a jumper on J1.

9 VDC Wall Converter (US 120 VAC Only):

Put a jack plug from a 9 VDC Wall Converter into the socket P17 (Center is positive). In this case, put a jumper on J28. When this jumper is fitted, you MUST NOT connect power by other means.

Powered by a Host System:

The evaluation board can also be connected to an external digital host processor board. Power can be routed from a host processor board to the Anadigm® evaluation board.

By default there is a jumper on J5 that allows power to be routed to the analog circuit on the board. This takes about 100 mA. In this condition, the board may power up in a high current state with the supply failing to reach 5 V. This happens because during power up, the analog circuit initially draws high current, which may cause the current limit of the supply to kick in, which in turn prevents the supply from reaching 5 V and causing the ICs to remain in a high current state. This can be fixed by removing the jumper from J5 and then reinserting it, or by increasing the current limit on the supply.

When the board is fully powered up there is a green LED (D3) at the top of the board which lights up. If the supply falls below about 4.4 V, there is a red LED (D4) also at the top of the board which lights up. If very low supply voltage is applied, LED (D4) will be dim or not light up.

1.2 Configuring the Evaluation Board

Once powered up, the board is ready to accept a configuration download.

1. In the default mode, configuration data can be downloaded from a PC running AnadigmDesigner®2 software, using the RS232 port. There is an on-board oscillator to provide the analog clock.
2. To make a self contained system without dependence on a PC, the board may be set into EPROM mode, using jumper J4. There are 2 EPROM sockets provided for this purpose - U3 for FPGA EEPROMs (e.g. Atmel AT17C65 65Kbit), and U4 for SPI EEPROMs (e.g. Atmel AT25080 8Kbit). There is a crystal on the board to drive the configuration process and the analog clock. Note that in EPROM mode, ACLK becomes an output to the EPROM and the analog clock is derived from the DCLK pin.
3. Lastly, the board may be configured by an external digital system of your own design, by disconnecting the digital interface on the board (J18) and connecting an external

digital system to socket P6 via a ribbon cable. The analog clock can be driven from this digital system or from the on-board oscillator module.

A Development License is required in order to download bitstream information to any external device: microcontroller, EEPROM, Flash, etc.

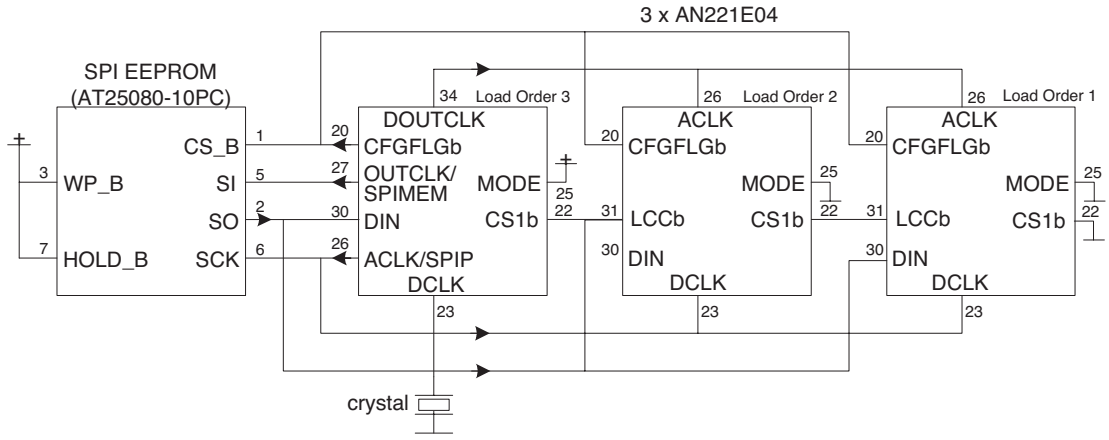


Figure 2 – Multiple FPAAs Configured from a Single SPI EEPROM

Figure 2 shows how three AN221E04 devices - one device on the main evaluation board and two devices on the daughter card - can be configured using a SPI EEPROM. Only MODE of the first device is connected high. This is because MODE=1 causes DCLK to be divided down internally for the EPROM which requires a slower clock on ACLK/SPIP.

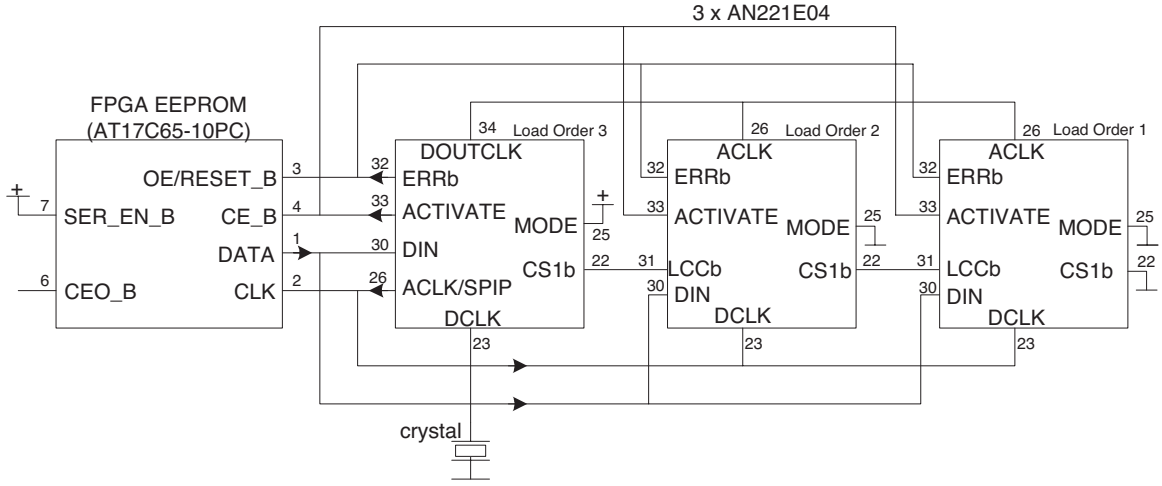


Figure 3 – Multiple FPAAs Configured from a Single FPGA EEPROM

Figure 3 shows the same configuration, using an FPGA EEPROM. There is an on-board oscillator module to provide the analog clock.

Figures 4 and 5 show the basic connections for single FPAA systems booted from a SPI EEPROM or an FPGA EEPROM respectively. The configuration interface of the AN221E04 automatically handles all the signaling requirements to either of these popular EEPROM families. The FPAA may be configured to simply boot itself from the attached non-volatile memory at power up.

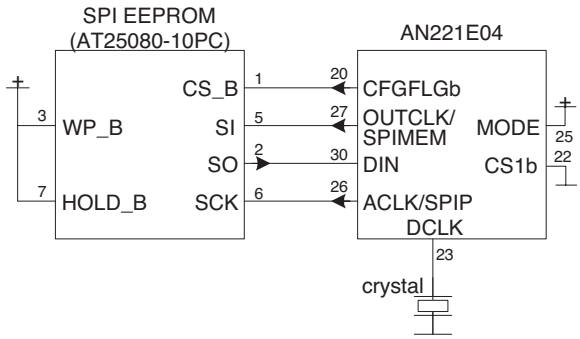


Figure 4 – A single FPAA Device with a Sample SPI EEPROM

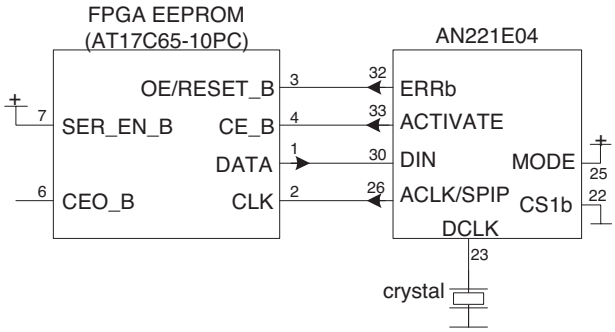


Figure 5 – A single FPAA Device with a Sample FPGA EEPROM

1.3 Using the I/O on the Evaluation Board

Header pins are provided for each pin of the AN221E04 device on the board. The AN221E04 can be isolated from the other active components on the board and connections made directly via these header pins. For convenience and ease of use, circuitry is placed on the board so input to the AN221E04 device can be provided in the following two additional ways:

1. Single-ended ground referenced signals can be input using the SMA connectors P11 and P12. By default, the SMA connector pins are connected to the differential input pins (pins I3P and I3N, I4PA and I4NA) of the AN221E04 device via two single-ended to differential converters (shown as U6 and U7 in Figure 6). The gain of these circuits is 1. The output is a differential signal whose amplitude is equal to the input signal amplitude, and whose common mode voltage will be VMR (nominally 2.0 V).

   Jumpers J9 and J10 can be lifted to isolate the U7 outputs from the AN221E04, and jumpers J7 and J8 can be lifted to isolate the U6 outputs from the AN221E04.

   If a differential signal is brought in from an AN221E04 on another board via the SMA inputs; jumpers can be used to bypass this single-ended to differential converter. Place the jumpers J7 and J8 in line rather than in parallel, and both the SMA connectors will be connected to the same differential input of the AN221E04 (I4PA and I4NA). The

jumpers should be taken off J31 and J32 to isolate the SMA connectors from the single-ended to differential converters. Figure 6 shows this circuit in detail.

2. A stereo jack plug from an audio source can also be connected into P18.

   Note you CANNOT drive input signals simultaneously from both the SMA connector as well as from the stereo jack.

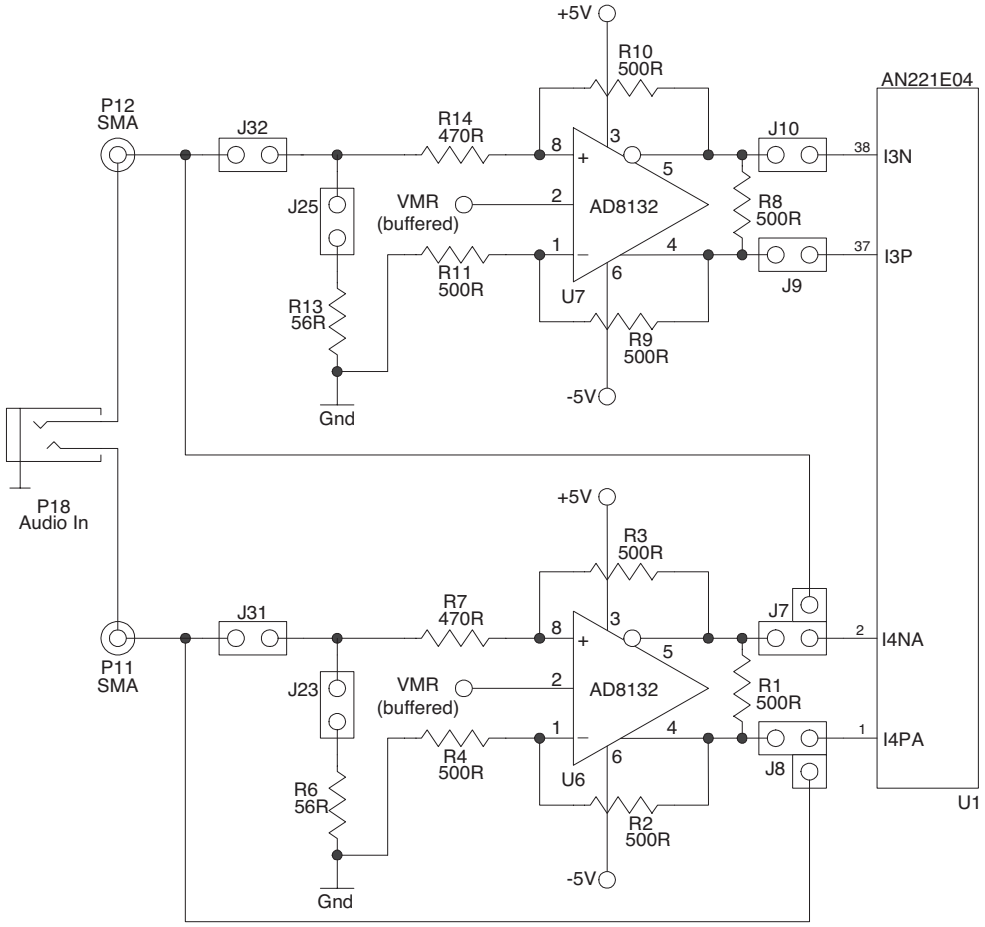


Figure 6 – Single-Ended to Differential Converters

In addition to the directly connected header pins, the output of the evaluation board is available via:

1. Single-ended ground referenced signals can be output on SMA connectors P9 and P10. By default the SMA connector P9 (P10) is connected to a differential to single-ended converter that is connected to O1P and O1N (O2P and O2N) of the AN221E04 device. There are two differential to single-ended converters on this board as shown in Figure 7.

   The two differential to single-ended converters can be bypassed in order to output a differential signal from the AN221E04 to an AN221E04 on another board via the SMA connectors. Place Jumpers J21 and J22 in the lower position to bypass the converters and connect O2P/O2N directly to the SMA connectors.

   The 4 jumper set J12 is one of a set of 3 jumpe sets: J12, J13, J14 (see Figure 9) - that allows the selection of signals to be fed to the differential to single-ended converters. Each converter can be driven by a choice of 3 differential pairs - one from the AN221E04 on the motherboard, two from the daughter card.

2. Alternatively P19 provides a stereo output to speakers or headphones.

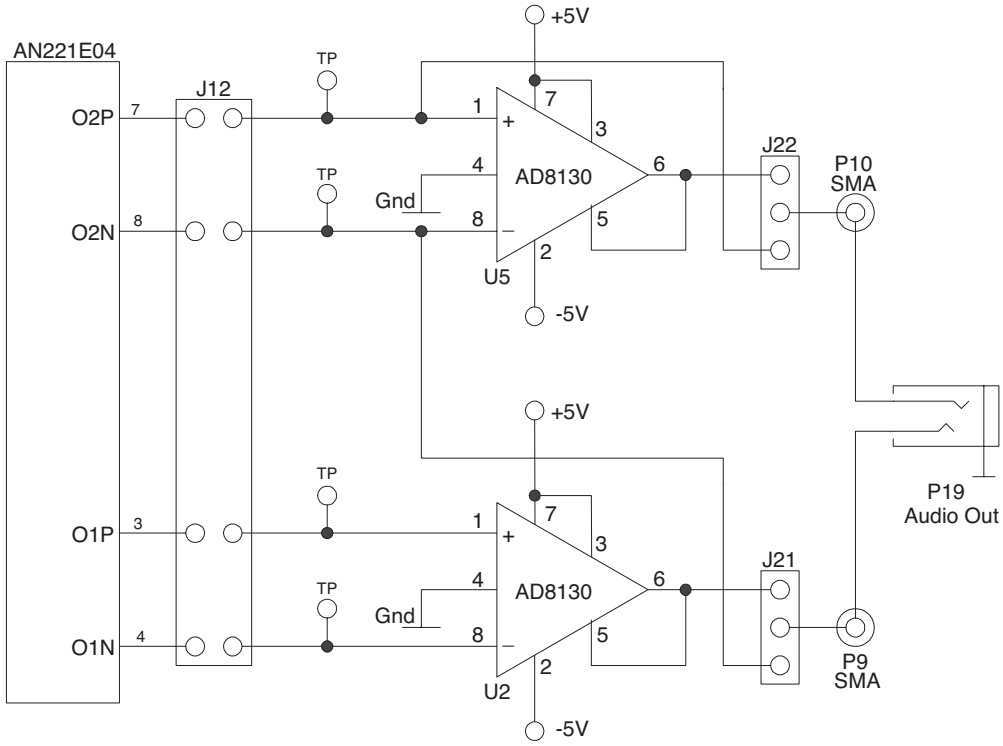


Figure 7 – Differential to Single-Ended Converters

1.4 Using the Daughter Card

There are two ANx2xE04 devices surface mounted onto the same side of a daughter card. 11 digital signals, 12 analog signals (6 differential pairs), plus 13 power and ground traces have been brought out to the edge so that the card can be plugged into a 36-way 0.1 inch pitch double-sided edge socket on the main evaluation board (motherboard). This socket has a polarizing key to prevent insertion of the daughter card the wrong way round. Figure 8 shows the digital signal connections on the daughter card.

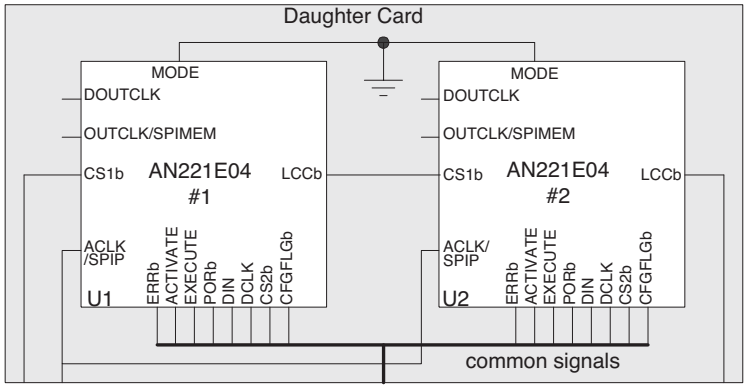


Figure 8 – Digital Signal Connections on Daughter Card

There are also 12 analog signals routed to the edge of the card. Figure 9 shows how the analog signals are connected between the 2 devices on the daughter card, and between the daughter card and motherboard (thick lines are differential pairs).

The buffers marked S2D are the single-ended to differential converters, those marked D2S are the differential to single-ended converters. Jumpers J12, J13 and J14 are used to select which outputs are connected to the differential to single-ended converters. Also shown in Figure 9 are the jumpers that allow disconnection of the S2D outputs from the AN221E04, jumpers that allow the disconnection of the input SMA connectors from the S2D inputs, jumpers that allow the connection of both input SMA connectors directly to I4PA and I4NA (i.e. bypass S2Ds), and jumpers that allow the connection of both output SMA connectors directly to O2P and O2N (i.e. bypass D2Ss).

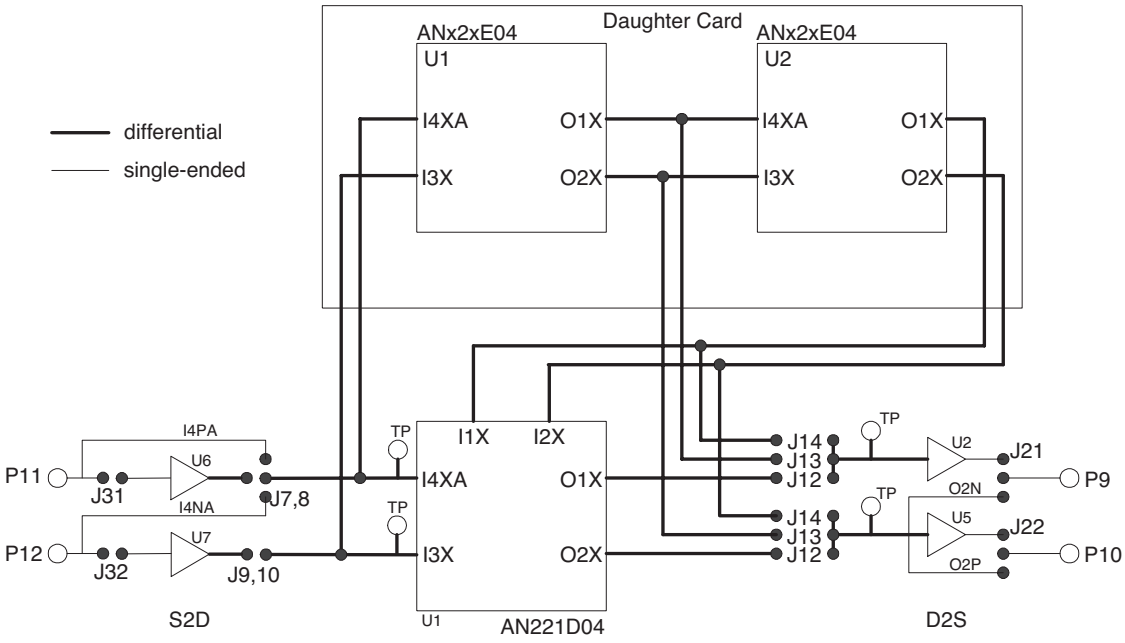


Figure 9 – Daughter Card to Motherboard Analog Connections

1.5 Expanding the Evaluation Board

The Anadigmvortex evaluation board can be expanded in two ways:

1. Insert an AN120D04-DAUGH, AN121D04-DAUGH, AN220D04-DAUGH, or an AN221D04-DAUGH daughter card into socket P8. This adds an extra two FPAA devices to the system.
2. Connect the main evaluation board to another via the expansion socket P7. There is no limit to the number of boards that can be daisy chained in this manner. Analog signals can be passed down the chain using SMA cables in either single-ended or differential mode.

When expanding the Anadigm evaluation system using a daughter card, keep in mind the following:

Use the correct number of devices within the AnadigmDesigner®2 software window. If all three devices are used (two on the daughter card and one on the motherboard), make sure three devices are placed in the software design window.

The correspondence between the devices in the AnadigmDesigner®2 software and the devices in the multichip evaluation system is determined by the load order set in the software (see the Daughter Card Quick Start Guide).

Load Order 1 corresponds to the daughter card device U1
Load Order 2 corresponds to the daughter card device U2
Load Order 3 corresponds to the device on the main evaluation board

Keep this load order in mind when designing your system. The load order can be set or modified from within the AnadigmDesigner®2 software by clicking on the load order number.

2 Jumper Settings

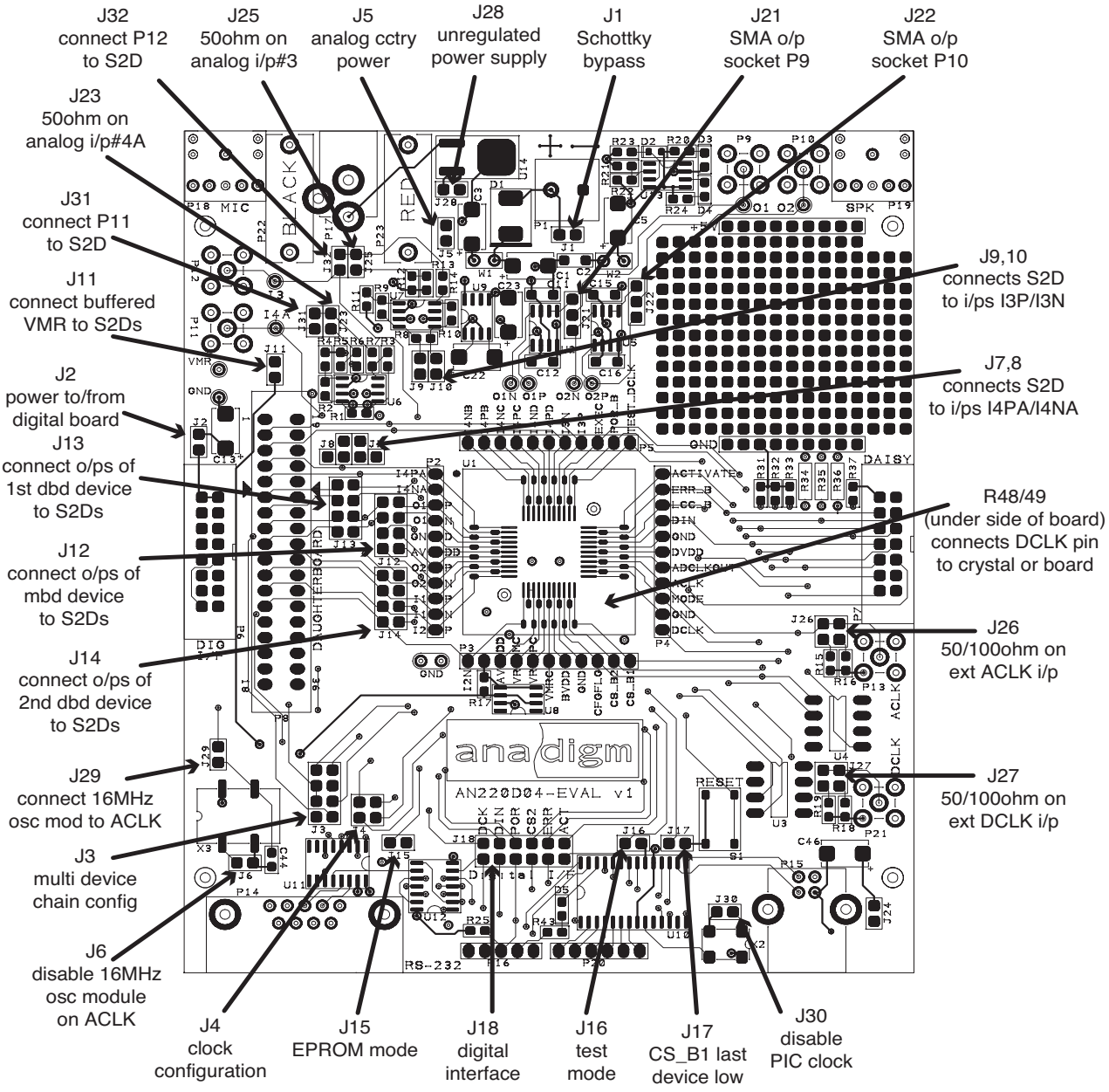


Figure 10 – Position of all the Jumpers On Board

Jumper	Function	Default State	Default Condition
J1	bypass Schottky protection diode	off	board protected
J2	power from digital board	on	power connected through P6
J3	multi device chain configuration		use mortherboard device only (Figure 11)
J4	clock configuration		non EPROM mode (Figure 12)
J5	analog circuitry power	on	analog circuitry powered up
J6	disable 16 MHz oscillator module	off	ACLK/SPIP driven by 16 MHz oscillator
J7,J8	connect S2D to I4PA/I4NA		use S2Ds on analog inputs (Figure 6)
J9,J10	connect S2D to I3P/I3N		use S2Ds on analog inputs (Figure 6)
J11	connect buffered VMR to S2D	on	use buffered VMR from chip
J12	connect outputs of motherboard device to D2S		use motherboard device (Figure 13)
J13	connect outputs of 1st daughter card device to D2S	all 4 off	no daughter card (Figure 13)
J14	connect outputs of 2nd daughter card device to D2S	all 4 off	no daughter card (Figure 13)
J15	EPROM mode	off	non EPROM mode
J16	test mode	off	not in test mode
J17	CS1b first device low	on	no expanded boards on P7
J18	digital interface		use digital interface
J21	connect O1P/O1N to D2S		use D2Ss on analog output (Figure 7)
J22	connect O2P/O2N to D2S		use D2Ss on analog output (Figure 7)
J23	50 ohm on analog input 4A	on	use 50 ohm termination on inputs (Figure 6)
J25	50 ohm on analog input 3	on	use 50 ohm termination on inputs (Figure 6)
J26	50/100 ohm on external ACLK/SPIP input	both off	external ACLK/SPIP input not used
J27	50/100 ohm on external DCLK input	both off	external DCLK input not used
J28	unregulated power supply	on	using unregulated supply
J29	16 MHz oscillator to ACLK/SPIP	on	ACLK/SPIP driven by 16 MHz oscillator
J30	disable PIC clock	off	use digital interface
J31	connect P11 SMA to S2D	on	use S2Ds on analog inputs (Figure 6)
J32	connect P12 SMA to S2D	on	use S2Ds on analog inputs (Figure 6)
R48	zero ohm resistor connects DCLK pin to rest of board	on	non EPROM mode
R49	zero ohm resistor connects crystal to DCLK pin	off	non EPROM mode

Table 1 — Jumper Function and Default Settings

J1 - Schottky Bypass

There is a Schottky diode on this board that protects the board from being powered up with the wrong polarity. This diode will typically drop about 0.2 V. If the user wishes to bypass this protection diode he should put a jumper on J1.

J2 - Power from Digital Board

If there is a digital board connected to the digital socket P6 via ribbon cable, a jumper on J2 connects the power supplies of the 2 boards.

J3 - Multi Device Chain Configuration

J3 is an 8 pin jumper block for configuring different chains of AN221E04 devices. Figure 11 shows the jumper positions to achieve the following configurations - motherboard device only, motherboard device followed by daughter card devices, bypass all devices to next analog board in the chain, daughter card devices only. Note that if using a daughter card only, the user must supply VMR (2 V) externally if he wishes to use the single-ended to differential converters.

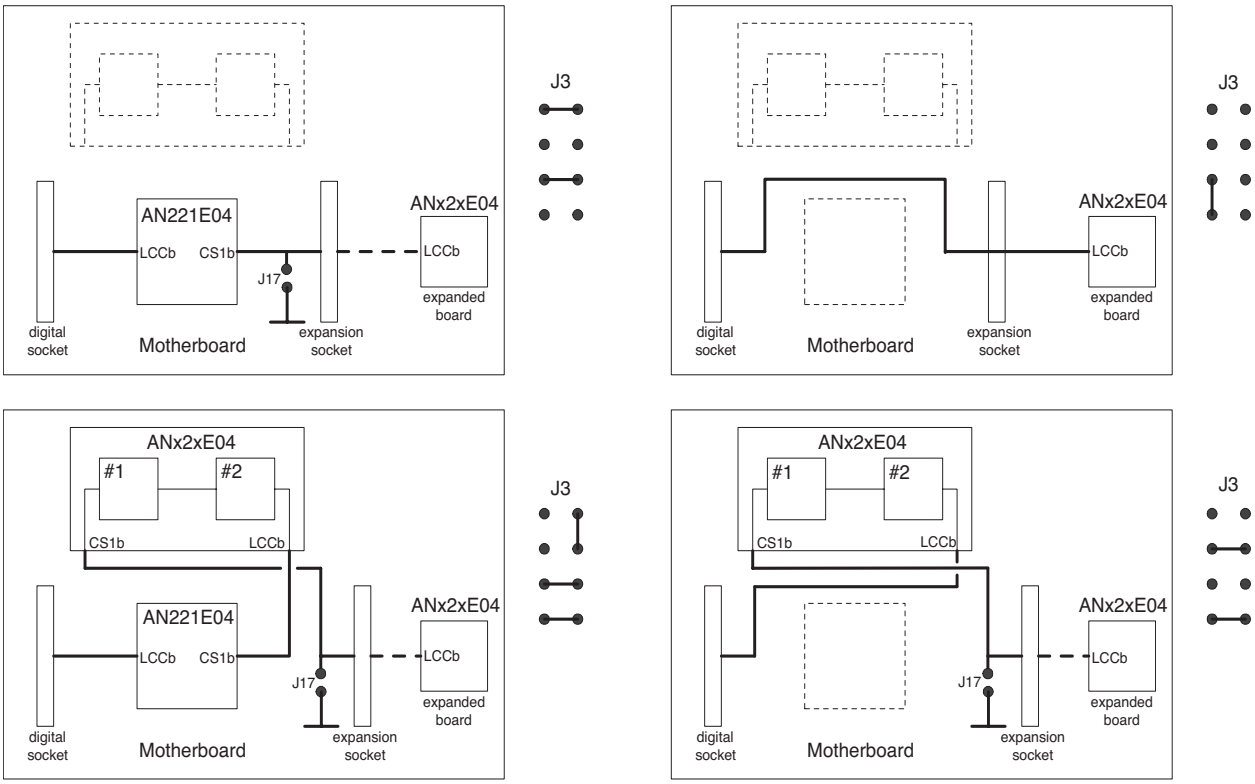
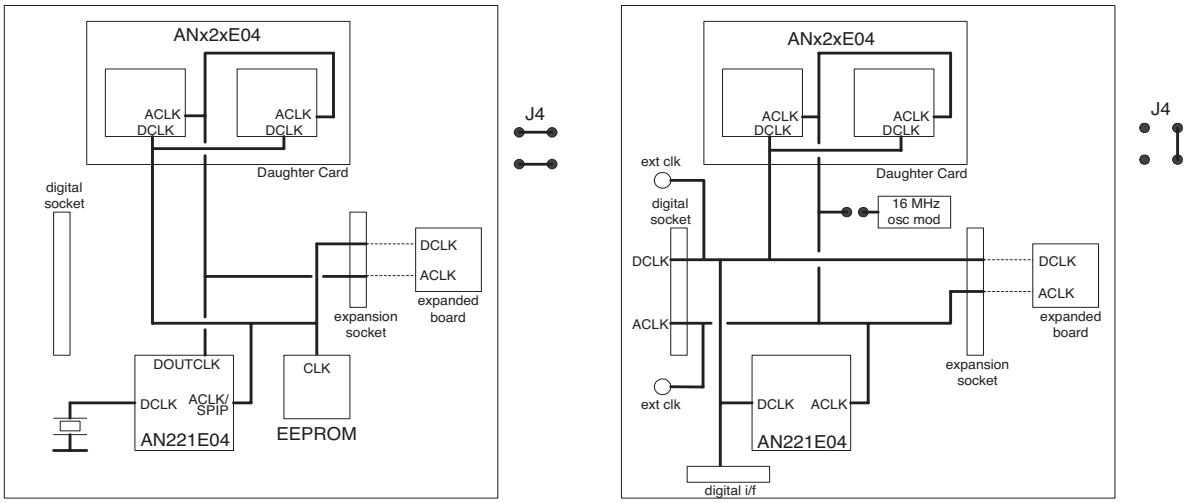


Figure 11 – J3 Jumper Settings for Different Chain Configurations

J4 - Clock Configuration

J4 is a 4 pin jumper block for configuring the clocks. Two jumpers placed horizontally allow the user to configure the AN221E04 from EEPROM. 1 jumper placed vertically on the right puts the board in non EEPROM mode (see Figure 12).



NOTES
1. configure motherboard device from EEPROM
2. configure motherboard device + daughter card from EEPROM

NOTES
1. configure motherboard device from digital socket/interface
2. configure motherboard device & daughter card from digital socket/interface
3. configure daughter card from digital socket/interface
4. ACLK can be supplied from the digital socket, externally, or from the 16 MHz osc module
5. DCLK can be supplied from the digital socket, externally, or from the digital interface (PIC)

Figure 12 – J4 Jumper Settings for Clock Configuration

J5 - Analog Circuitry Power

A jumper on J5 powers up all of the on-board analog circuitry. This circuitry consists of a VMR buffer, a -5 V supply, 2 single-ended to differential converters (these also level-shift from ground to VMR), and 2 differential to single-ended converters (these also level-shift from VMR to ground). All of this circuitry takes about 100ma.

J6 - ACLK/SPIP 16 MHz Oscillator Module Disable

A jumper on J6 disables the 16 MHz oscillator module used to drive ACLK/SPIP. If jumper J6 is fitted, jumper J29 should be left off to disconnect the oscillator module from ACLK/SPIP.

J7, J8 - S2D Converter to I4PA & I4NA

These jumpers connect the SMA connector P11 to pins I4PA and I4NA of the AN221E04 via a single-ended to differential converter. A jumper must be placed on both J7 and J8 (in parallel, vertically on the board) to do this. If the jumpers are placed in line (horizontally on the board); SMA connectors P11 and P12 will be connected directly to I4PA and I4NA respectively, bypassing the S2D converter. This would be done in order to input a differential signal from an AN221E04 on another board via the SMA cable. Note that in this situation, the user should also remove jumpers J31 and J32. It is important that the user should leave jumpers J7 and J8 open if he wishes to apply signals directly to I4PA and I4NA via the AN221E04 header pins. Figure 13 illustrates how the analog signals are routed.

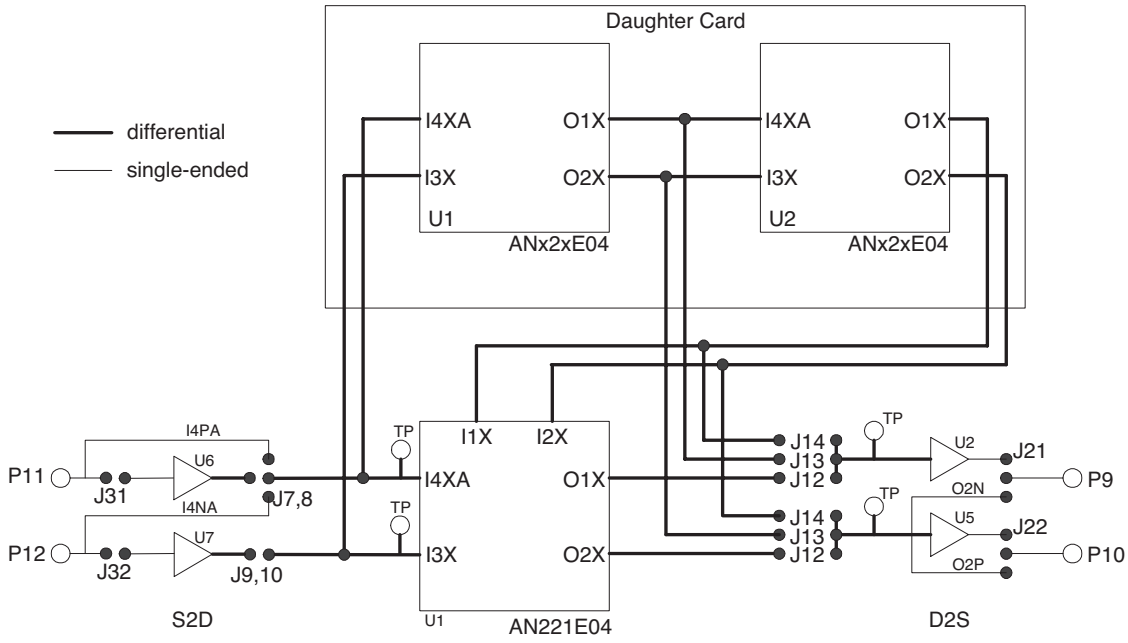


Figure 13 – Analog Signal Routing

J9, J10 - S2D Converter to I3P & I3N

These jumpers connect the SMA connector P12 to pins I3P and I3N of the AN221E04 via a single-ended to differential converter. A jumper must be placed on both J9 and J10 (vertically on the board) to do this. It is important that the user should leave these jumpers open if he wishes to apply signals directly to I3P and I3N via the AN221E04 header pins.

J11 - Select Buffered VMR

A jumper on J11 connects the VMR buffer to the S2D converters for the purpose of level-shifting incoming single-ended signals. VMR can be monitored at the VMR test point close to this jumper. If the user wishes to apply his own VMR, he should remove this jumper and apply a voltage directly to the VMR test point.

J12, 13, 14 - Output Select to D2S

J12, J13 and J14 each consist of 8 pins arranged in 4 pairs that take 4 jumpers horizontally. Only one of J12, J13 and J14 should be populated with jumpers at any time. J12 connects the outputs of the motherboard device to the differential to single-ended converters e.g. when using only a motherboard device or when using a chain of 3 devices consisting of the daughter card followed by the motherboard device. J13 should be used if the outputs of the first daughter card device are required to be output through the differential to single-ended converters. J14 should be used if the outputs of the second daughter card device are required to be output through the differential to single-ended converters. Figure 13 illustrates how the analog signals are routed.

J15 - EPROM Mode Motherboard

A jumper should be placed on J15 for EPROM mode. Note that in EPROM mode, ACLK becomes an output to the EPROM and the analog clock is derived from the DCLK pin.

J16 - Test Mode

A jumper should be placed on J16 to put the (motherboard) AN221E04 device into test mode. Note that there is no option for putting the daughter card devices into test mode.

J17 - CS1b First Device

The first AN221E04 in the chain (furthest down the chain) must have it's CS1b pin tied hard low, therefore the user should put a jumper on J17 if there is no card connected to the expansion socket (i.e. there are no cards further down the chain). The ANx20E04 device with CS1b tied low will be the first device to be loaded.

J18 - Digital Interface

This set of 6 jumpers connects the AN221E04 to the on-board digital interface. This interface allows configuration of the AN221E04 using the RS232 interface. These jumpers should not be fitted if there is a digital board connected to the digital socket P6.

J21 - SMA Output Socket P9

The user should place a jumper in the upper position on the board to connect SMA connector P9 to the differential to single-ended converter that is connected to O1P and O1N of the AN221E04. The user should place the jumper in the lower position to connect SMA connector P9 directly to output O2N, bypassing the differential to single-ended converter. This would be done in conjunction with J22 in order to output a differential signal from the AN221E04 to an AN221E04 on another board via SMA cable. Figure 13 illustrates how the analog signals are routed.

J22 - SMA Output Socket P10

The user should place a jumper in the upper position on the board to connect SMA connector P10 to the differential to single-ended converter that is connected to O2P and O2N of the AN221E04. The user should place the jumper in the lower position to connect SMA connector P10 directly to output O2P, bypassing the differential to single-ended converter (see Figure 7). This would be done in conjunction with J21 in order to output a differential signal from the AN221E04 to an AN221E04 on another board via SMA cable. Figure 13 illustrates how the analog signals are routed.

J23 - 50 ohm on Analog Input 4A

A jumper on J23 connects a 50 ohm resistor to ground on the analog input 4A (P11). Note that without this jumper, the input impedance to the S2D converter is 500 ohm.

J25 - 50 ohm on Analog Input 3

A jumper on J25 connects a 50 ohm resistor to ground on the analog input 3 (P12). Note that without this jumper, the input impedance to the S2D converter is 500 ohm.

J26 - 50/100 ohm on External ACLK/SPIP Input

This jumper serves a dual role. If the user is supplying ACLK/SPIP externally from a 50 ohm signal generator, he should place 2 jumpers vertically onto J26 to provide 50 ohm termination. The second role of this jumper is as follows - if the user is chaining 2 or more boards with ACLK/SPIP supplied from a board at one end of the chain, he should place a single jumper vertically on J26 of the board at the other end of the chain. This terminates the clock line and prevents reflections along the chain.

J27 - 50/100 ohm on External DCLK Input

This jumper serves a dual role. If the user is supplying DCLK externally from a 50 ohm signal generator, he should place 2 jumpers vertically onto J26 to provide 50 ohm termination. The second role of this jumper is as follows - if the user is chaining 2 or more boards with DCLK supplied from a board at one end of the chain, he should place a single jumper vertically on J26 of the board at the other end of the chain. This terminates the clock line and prevents reflections along the chain.

J28 - Unregulated Power Supply

A jumper on J28 allows the user to connect an unregulated power supply to the board via the jack plug socket P17. When this jumper is fitted, the user should not connect power by any other means than the jack plug socket.

J29 - 16 MHz Oscillator Module to ACLK/SPIP

A jumper on J29 connects the 16 MHz oscillator module to ACLK/SPIP. Note that when using the oscillator module, jumper J6 should be left off to enable the oscillator.

J30 - Disable PIC Clock

A jumper on J30 disables the 24 MHz oscillator module that supplies the clock to the PIC. This jumper should be fitted when the user is not using the on-board digital interface and he wishes to reduce the board's power consumption.

J31, J32 - Connect P11 & P12 to S2D Converters

Removing the jumpers from J31 and J32 disconnects the SMA connectors P11 and P12 from the S2D converters. The user should do this if he wishes to connect the SMA connectors P11 and P12 directly to pins I4PA and I4NA of the AN221E04 (see J7, 8) and he wants a high input impedance. This would be recommended if the differential signal coming in on P11 and P12 were coming directly from another AN221E04.

R48, R49 - DCLK Source

R48 and R49 are 2 resistor footprints on the bottom of the board underneath the AN221E04. Either one of these (not both) should be populated with a zero ohm resistor (or short length of wire). If the user wishes to connect the crystal to the DCLK pin, he should put a resistor on R49. If he wishes to connect the DCLK pin to the rest of the board, he should put a resistor on R48.

3 Typical Board Configurations

	Default State	EPROM Mode	External Digital Interface	No Analog Circuitry	Daughter Only 2 Devices	Daughter + Mother 3 devices	External Clocks	Expanded Board First Board	Expanded Board Last Board
J1	off	off	off	off	off	off	off	off	off
J2	on	off	on	off	off	off	off	off	off
J3									
J4									
J5	on	on	on	off	on	on	on	on	on
J6	off	on	off	off	off	off	off	off	on
J7,J8									
J9,J10									
J11	on	on	on	off	off	on	on	on	on
J12									
J13									
J14									
J15	off	on	off	off	off	off	off	off	off
J16	off	off	off	off	off	off	off	off	off
J17	on	on	on	on	on	on	on	off	on
J18									
J21									
J22									
J23	on	on	on	off	on	on	on	on	on
J24	off	off	off	off	off	off	off	off	off
J25	on	on	on	off	on	on	on	on	on
J26									
J27									
J28	on	off	off	off	off	off	off	off	off
J29	on	off	on	on	on	on	off	on	off
J30	off	on	on	off	off	off	off	off	on
J31	on	on	on	off	on	on	on	on	on
J32	on	on	on	off	on	on	on	on	on
R48	on	off	on	on	on	on	on	on	on
R49	off	on	off	off	off	off	off	off	off

Default State Setting

On-board digital interface allows configuration using RS-232 sockets. On-board analog circuitry allows use of single-ended ground-referenced signals.

EPROM Mode Setting

This self-contained mode allows configuration from EEPROM. A crystal on the AN221E04 means that no other clock is required. The on-board digital interface is disconnected and its clock disabled to reduce noise. Note that in EPROM mode, ACLK/SPIP becomes an output to the EPROM and the analog clock is derived from the DCLK pin.

External Digital Interface Setting

The user wishes to use his/her digital interface via the digital interface socket P6. The on-board digital interface is disconnected and its clock disabled to reduce noise.

No Analog Circuitry Setting

The user doesn't wish to use the on-board analog circuitry. The SMA connectors P11 and P12 are disconnected from the single-ended to differential converters and connected directly to I4PA/I4NA. The 50 ohm terminations are disconnected from P11 and P12 to allow connection to the analog outputs of another AN221E04.

The SMA connectors P9 and P10 are disconnected from the differential to single-ended converters and connected directly to O2P/O2N.

Daughter Card Only - 2 Devices Setting

A two-device system using a daughter card and NO motherboard device.

Daughter Card + Motherboard - 3 Devices Setting

A three-device system using a daughter card and motherboard device.

External Clocks Setting

The user wishes to supply an external clock to either DCLK or ACLK/SPIP from a 50 ohm source.

Expanded Board - First board

This setting is for a system containing multiple devices by daisy-chaining boards via the expansion socket P7. This shows the jumper settings for the first board in the chain; whose digital interface is being used to program the chain.

Expanded Board - Last board

This setting is for a system containing multiple devices by daisy-chaining boards via the expansion socket P7. This shows the jumper settings for the last board in the chain; which is being programmed from the first board.

4 Electrical and Mechanical Specifications

The purpose of the evaluation board is to provide engineers with a simple platform to evaluate the features and capabilities of the Anadigmvortex FPAA device(s). The board is not intended for direct use within a commercial product. All evaluation boards are electrically tested prior to shipment. The evaluation board is not a qualified product, but is an engineering tool meant for the purpose stated above.

These specifications are for the external peripheral circuitry on the evaluation board. Direct connection to the FPAA can also be made using the header pins which surround the device – in which case please refer to the specifications for the AN221E04 device available in the data sheet.

4.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DC Power Supply	Banana Jack P22 & P23	4.75	5.00	5.25	V	DC Voltage Only J28 absent & J1 fitted
DC Power Supply	Banana Jack P22 & P23	4.95	5.20	5.45	V	DC Voltage Only J28 absent & J1 absent
DC Power Supply	Screw Terminal P1	4.75	5.00	5.25	V	DC Voltage Only J28 absent & J1 fitted
DC Power Supply	Screw Terminal P1	4.95	5.20	5.45	V	DC Voltage Only J28 absent & J1 absent
DC Power Supply	2.1mm Jack P17	8.00	9.00	12.00	V	DC Voltage Only – J28 Fitted (Center pole is positive, Outer sleeve is ground)
Input Voltage - Analog Input 3 - Analog Input 4a - Audio Socket	 SMC Jack P12 SMC Jack P11 Jack P18	-0.5	–	5.5	V	 R_{in} = 50 Ω R_{in} = 50 Ω CD Player or similar signal source expected.
Output Voltage - Analog Output 1 - Analog Output 2 - Audio Socket	P9 P10 Jack P19	-0.5	–	5.5	V	Active speakers or high impedance headphones are the expected load.
Input Voltage - RS-232	9 Pin D-Type P14	Vss - 0.5	–	Vdd + 0.5	V	Standard RS-232 signal levels are expected.
Input/Output Voltage	P6 & P7	–	–	–		Vdd and Vss refer to the AN221E04 device supplies.
Input Voltage - External Clocks	ACLK - P13 DCLK - P21	Vss - 0.5	–	Vdd + 0.5	V	Standard 5 V logic signals are expected.
Operating Temp.	T_{op}	10	–	50	°C	Ambient Operating Temperature
Storage Temp.	T_{stg}	-20	–	70	°C	Ambient Storage Temperature

4.2 Recommended Operation Conditions

Parameter	Symbol	Typ	Unit	Comment
DC Power Supply	Banana Jack P22 & P23	5.00	V	DC Voltage Only J28 absent & J1 fitted
DC Power Supply	Banana Jack P22 & P23	5.20	V	DC Voltage Only J28 absent & J1 absent
DC Power Supply	Screw Terminal P1	5.00	V	DC Voltage Only J28 absent & J1 fitted
DC Power Supply	Screw Terminal P1	5.20	V	DC Voltage Only J28 absent & J1 absent
DC Power Supply	2.1mm Jack P17	9.00	V	DC Voltage Only – J28 Fitted (Center pole is positive, Outer sleeve is ground)
Input Voltage - Analog Input 3 - Analog Input 4a - Audio Socket	 SMC Jack P12 SMC Jack P11 Jack P18	< 3.00	V	 R_{in} = 50 Ω R_{in} = 50 Ω CD Player or similar signal source expected.
Output Voltage - Analog Output 1 - Analog Output 2 - Audio Socket	P9 P10 Jack P19	< 3.00	V	Active speakers or high impedance headphones are the expected load.
Input Voltage - RS-232	9 Pin D-Type P14	–	V	Standard RS-232 signal levels are expected.
Input/Output Voltage	P6 & P7	5.00		Vdd and Vss refer to the AN221E04 device supplies.
Input Voltage - External Clocks	ACLK - P13 DCLK - P21	5.00	V	Standard 5 V logic signals are expected.
Operating Temp.	T_{op}	25	°C	Ambient Operating Temperature
Storage Temp.	T_{stg}	25	°C	Ambient Storage Temperature

4.3 Power Consumption

Parameter	Connection	Min	Typ	Max	Unit	Comment
Quiescent Power[a]	Power supply connections: P1, P17, P22, P23	0	50	60	mA	25 °C is assumed for all parameters. Note – Connect only a single supply at any time.
Nominal Power[b]		–	250	300	mA	
Maximum Power[c]		–	320	350	mA	
Maximum Power[d]		–	700	750	mA	
Maximum Peak Current[e]		–	1200	–	mA	

a. Quiescent power consumption, 16 MHz oscillator module (X3) connected to the AN221E04 device. No CAMs programmed. External circuitry powered down (Jumper J5 absent).
b. Nominal power consumption, 16 MHz oscillator module (X3) is connected to the AN221E04 device. All peripheral circuitry is active, one input cell active, one output cell active, two gain stages and one filter CAM.
c. Maximum power consumption, 16 MHz oscillator module (X3) is connected to the AN221E04 device. 4 analog multipliers, 4 inputs and 2 outputs active.
d. Same as c, except daughter card fitted and loaded with 8 analog multipliers.
e. Inrush current at switch on.

4.4 Mechanical

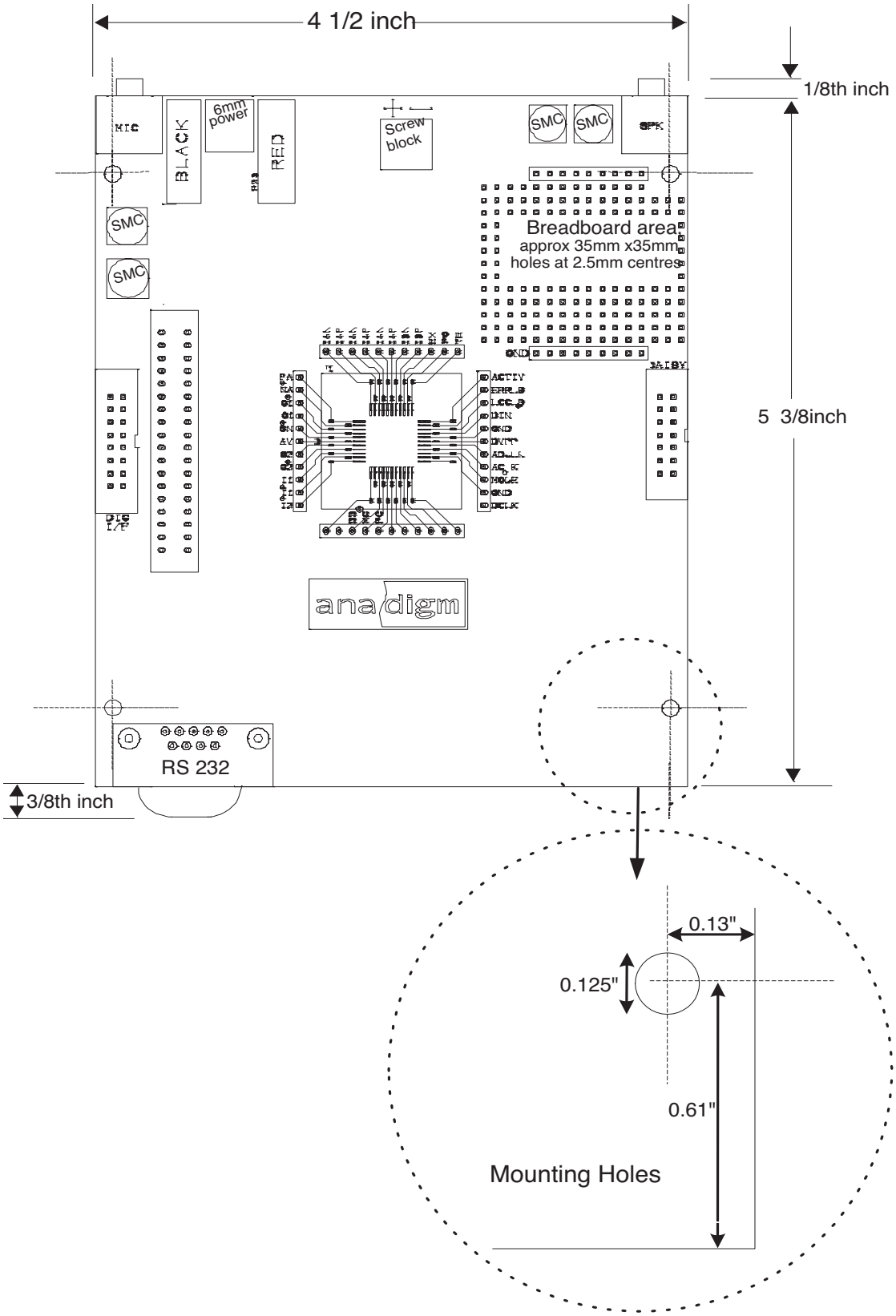
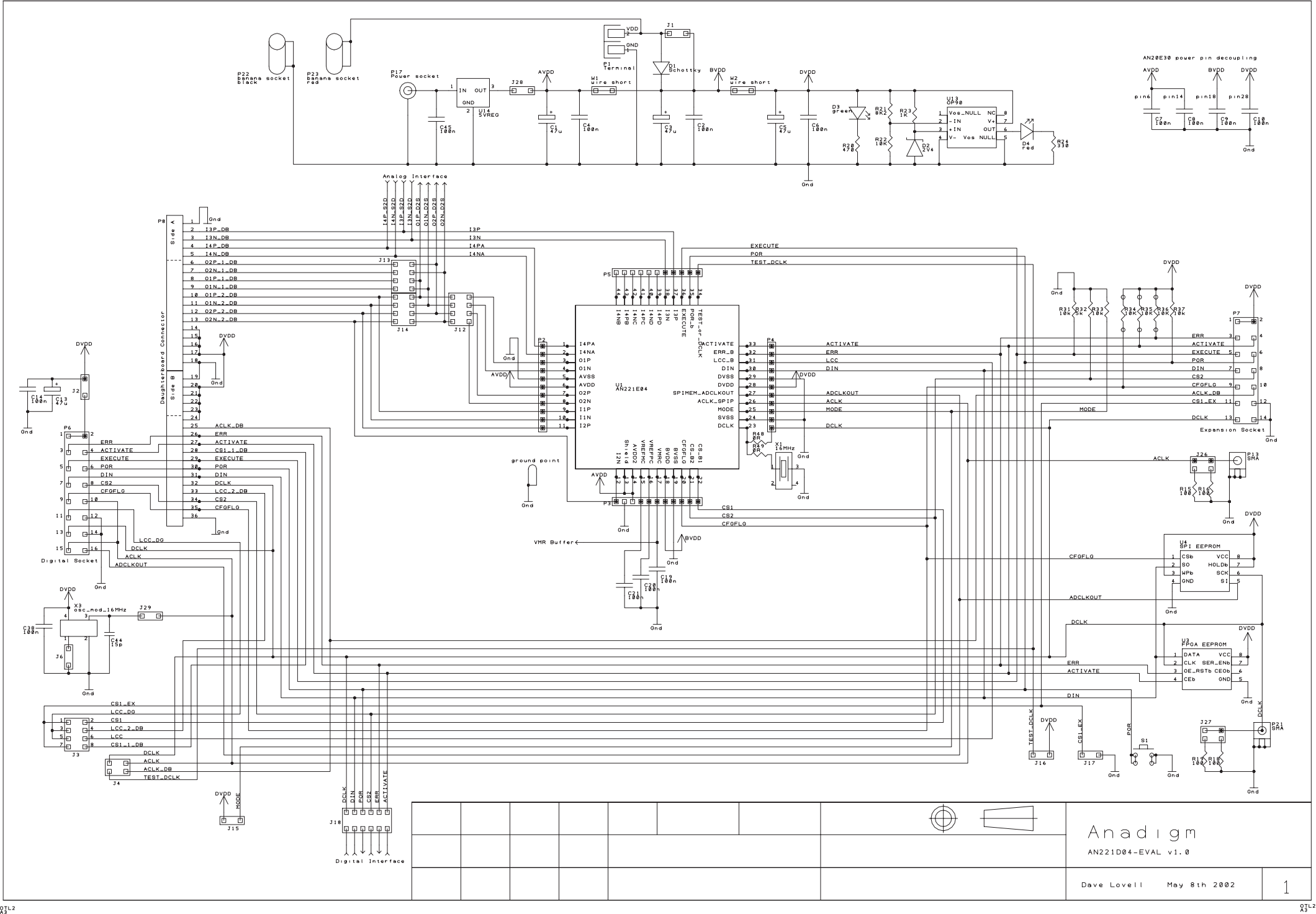


Figure 14 – Mechanical Outline for the AN221D04 Motherboard

Appendix – Evaluation Board Schematics



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AN221D04-EVAL v1.0

Dave Lovell May 8th 2002

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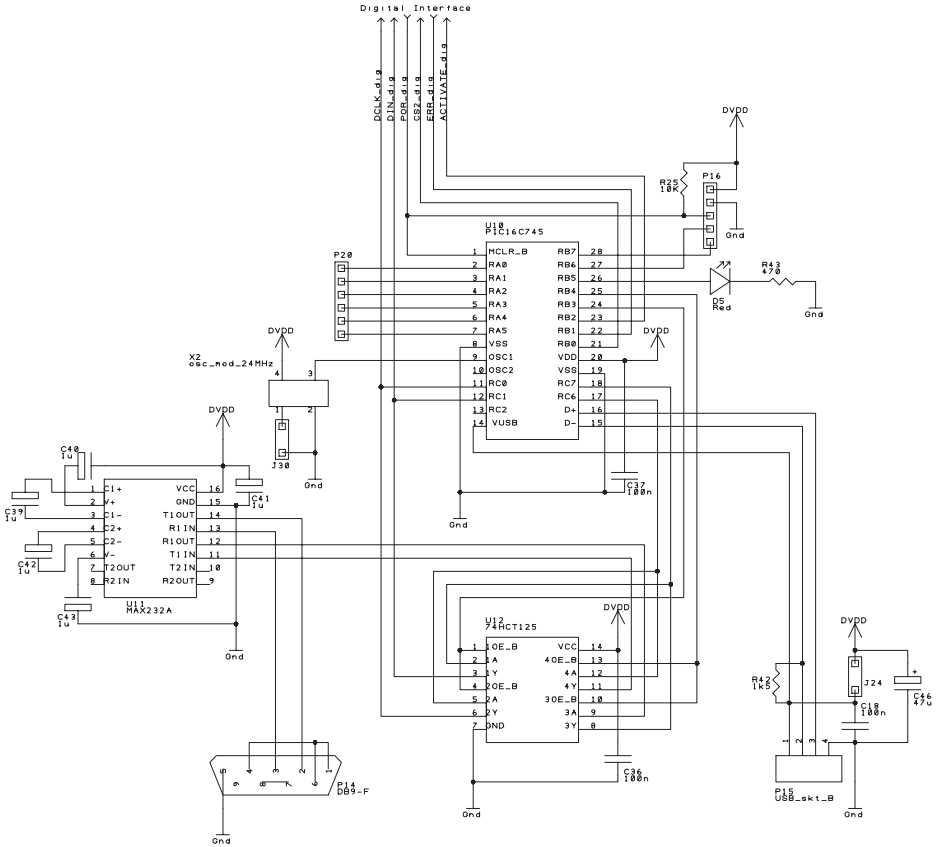

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AN221D04-EVAL v1.0 Digital Circuitry

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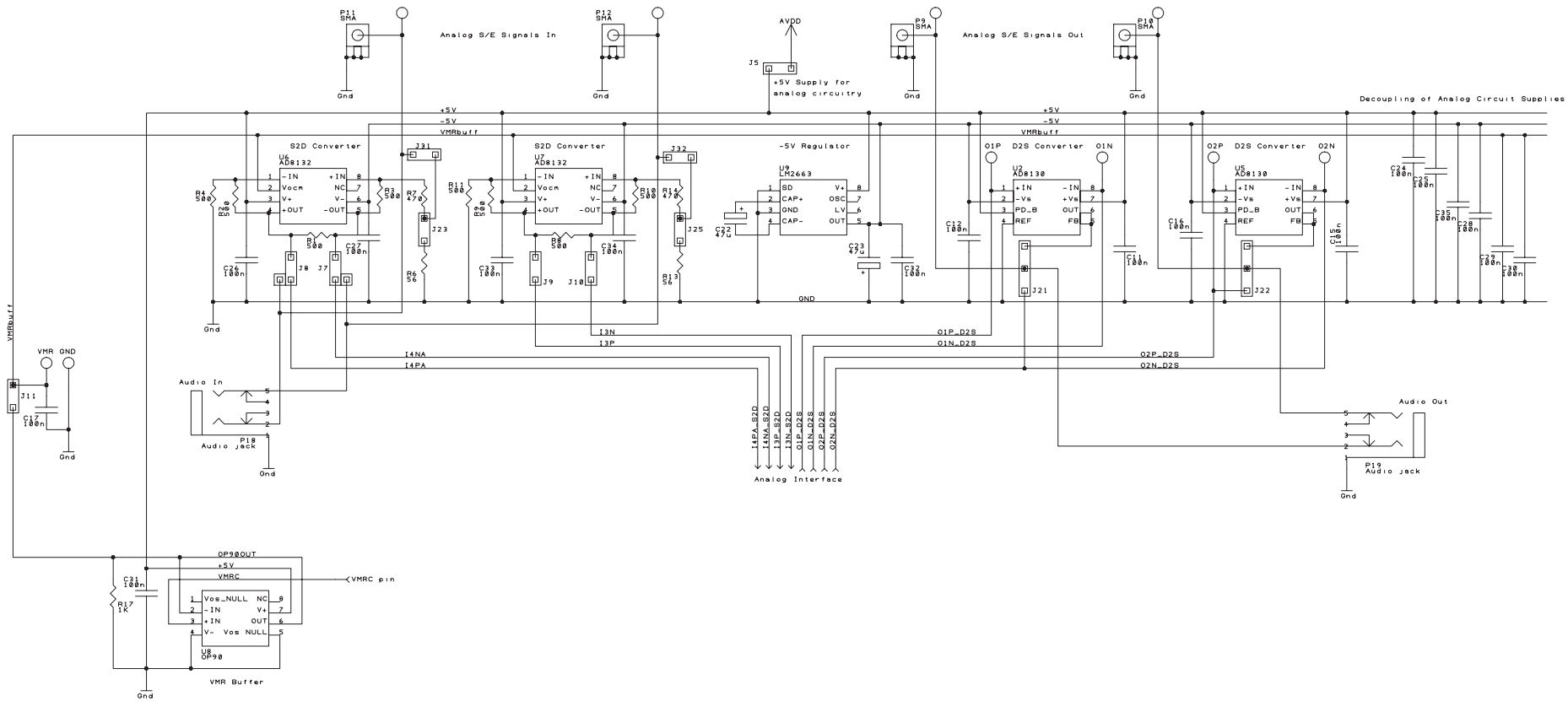

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